ISL35111 Evaluation Board User Guide

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Introduction to the ISL35111DRZ-EVALZ Evaluation Kit

The ISL35111 Evaluation Board is a stand-alone printed circuit board developed to evaluate the performance of the Intersil ISL35111 Driver.

The evaluation kit includes:

- ISL35111 evaluation board
- Power cable

The key features of the Evaluation board are:

- ISL35111 IC.
- Connection to external 5V power supply.
- On board DC/DC converter that provides the 1.2V supply to the IC.
- On board de-emphasis selection through a set of headers.
- SMA connectors to access differential input and output.

Operation of the ISL35111 Evaluation Board

This section describes how to simply setup your ISL35111 evaluation board making sure proper power is applied, describing connection to high speed RF input and output and finally describing how to easily set the driver's de-emphasis. The board is shown in Figure 1.

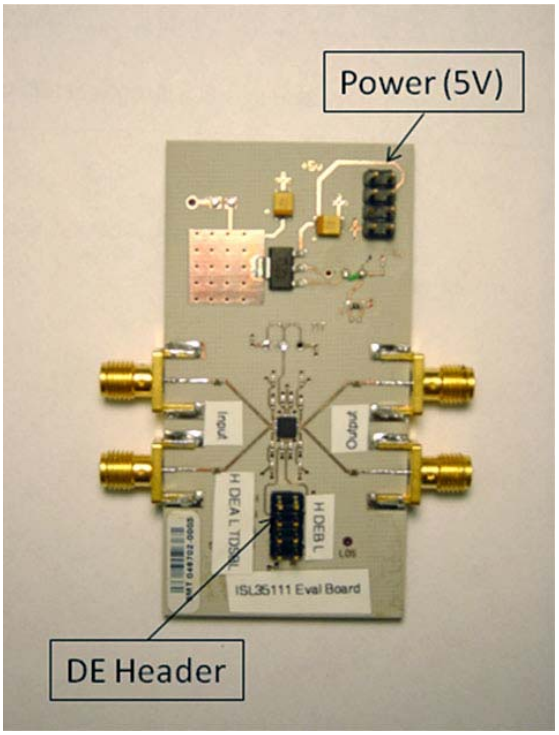

FIGURE 1. ISL35111 EVALUATION BOARD

Power Supply

The board needs to be powered by an independent external 5.0V power supply via the power header located at the top of the board using the power cable provided. The typical current consumption of the board is 48mA when no signal is applied and 65mA when a signal applied to the board input.

High Speed Data I/O Interface Connectors

Intersil Driver is intended to be used at the transmit end of a lossy channel (board trace or twinax cable). The input SMA connectors should be connected to the signal source. The output SMA connectors should be connected to the cable or PCB trace input. We recommend using length or phase matched RF cables in order to preserve the fidelity of the differential signal. Make sure proper torque is applied on the SMA connectors for reliable measurements and in order to prevent damage to the connectors.

De-emphasis Setting Control

The ISL35111 offers seven different levels of output de-emphasis. The amount of de-emphasis varies from 0dB (level 0) to 4dB (level 6). The de-emphasis level is set by positioning jumpers on header JMP1. DEA and DEB can each be set to one of three values (High, Low, Open) depending on jumpers position as illustrated in Figure 2. Table 1 describes jumper positions to achieve the various de-emphasis levels. As an example, Figure 2 depicts the jumper position to achieve de-emphasis level 5 (DEA Low and DEB High).

TABLE 1. JUMPER POSITIONS FOR BOOST SETTINGS

DEA	DEB	DE LEVEL	DE (dB)
No Jumper	No Jumper	0	0
No Jumper	Jumper to Low	1	0.6
No Jumper	Jumper to High	2	1.1
Jumper to Low	No Jumper	3	1.6
Jumper to Low	Jumper to Low	4	2.3
Jumper to Low	Jumper to High	5	3
Jumper to High	No Jumper	6	4

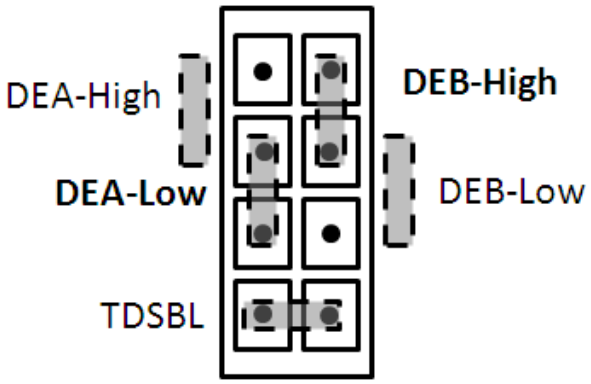

FIGURE 2. JUMPER CONFIGURATION FOR DE-EMPHASIS LEVEL 5

FIGURE 3. SETUP DIAGRAM

Transmit Disable

The output of the evaluation board can be disabled by inserting a jumper across the bottom 2 pins of header JMP1 as illustrated in Figure 2. In that mode, the IC enters a low power mode. For normal operation, no jumper must be present in this location.

Loss Of Signal (LOS) Test Point

During normal operation, the Loss Of Signal Test Point will be low (< 250mV). If the input signal to the evaluation board is turned off then the output of the evaluation board will also be turned off and the LOS Test Point will be high (>1V).

Baseline Performance

Performance is measured using the setup illustrated in Figure 3. The differential signal from the pattern generator is launched into the evaluation input and its output is visualized with a scope to determine jitter and de-emphasis.

Figure 4 shows the board output at 10.3125Gbps using a PRBS31 pattern for minimum and maximum de-emphasis settings. Figure 5 shows the signal in Figure 4B after it has traveled down 22 inches of FR4-08.

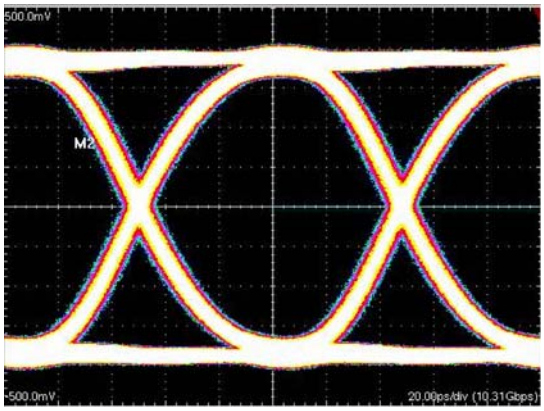

FIGURE 4A.

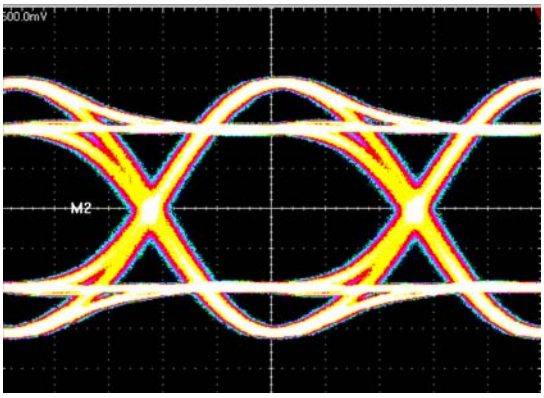

FIGURE 4B.

FIGURE 4. ISL35111 DRIVER OUTPUT EYE DIAGRAMS FOR DE-EMPHASIS A) LEVEL 0, AND B) LEVEL 6

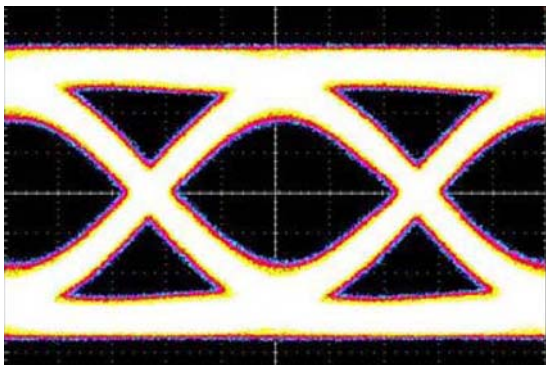

FIGURE 5. EYE DIAGRAM AFTER A 22IN FR4-08 TRACE USING DE-EMPHASIS LEVEL 6 FOR A 10.3125Gbps PRBS31 SIGNAL

Schematic

The ISL35111 evaluation board schematic is shown in Figure 6.

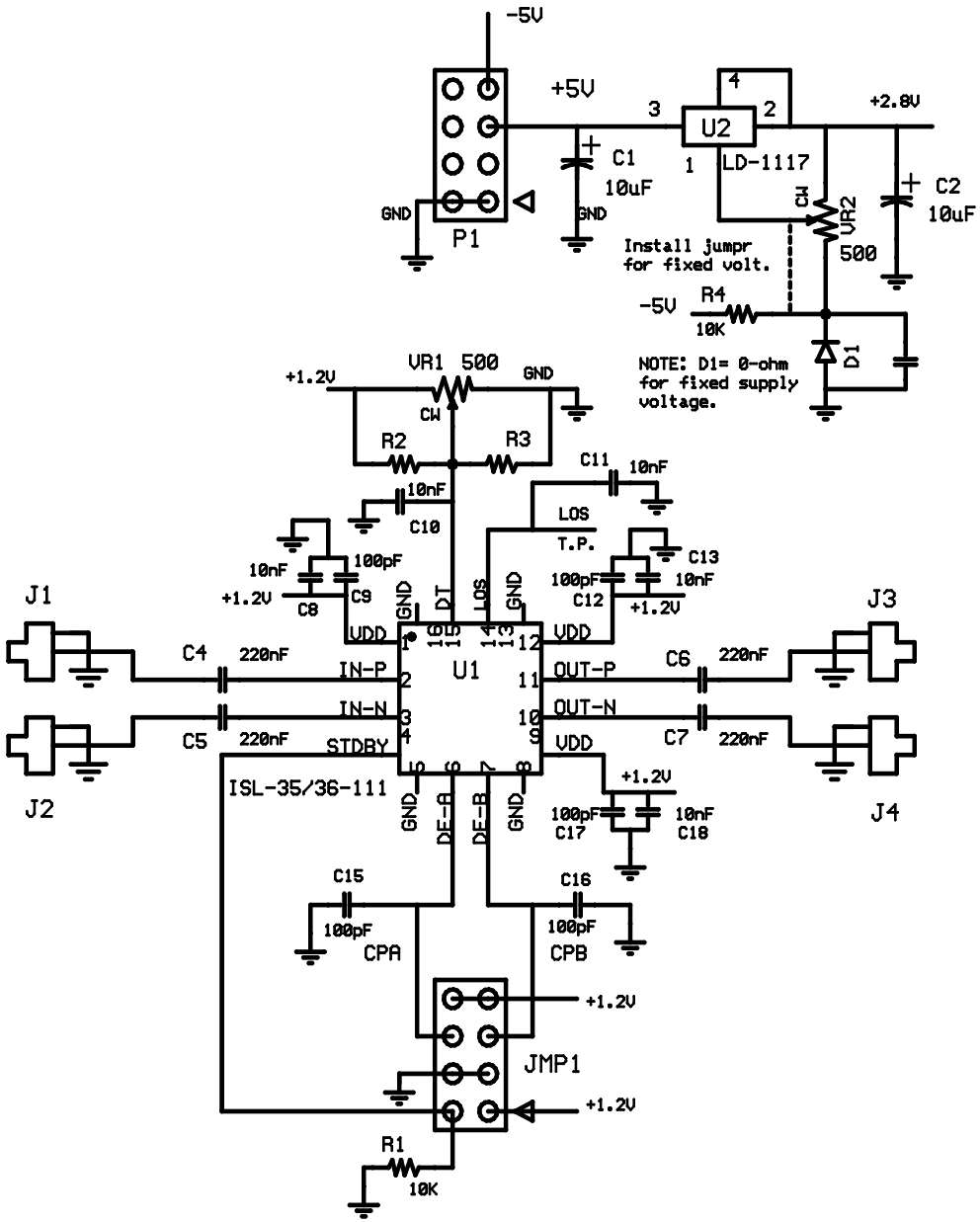

FIGURE 6. ISL35111 EVALUATION BOARD SCHEMATIC

About Intersil

Intersil specializes in analog components that improve the performance and functionality of electronic equipment. By removing channel impairments and interference noise, Intersil achieves dramatic improvements in high-speed channel performance across multiple industry segments, thus greatly enhancing the functionality of end-user applications.

Intersil is based in Santa Clara, California with additional sales and engineering centers in Atlanta, Georgia and Tokyo, Japan.

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