RF2948B

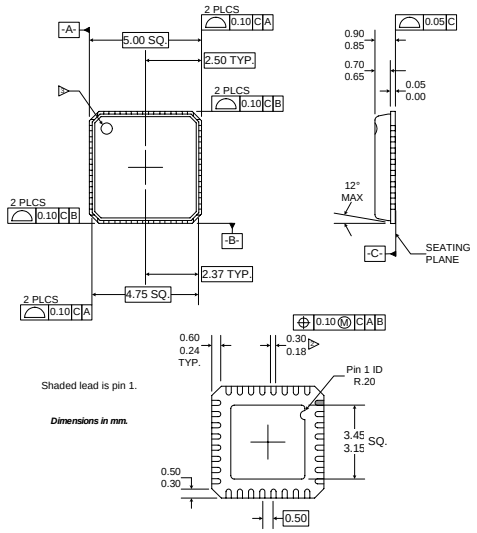
2.4GHz SPREAD-SPECTRUM TRANSCEIVER

Typical Applications

- IEEE 802.11b WLANs
- Wireless Residential Gateways
- Secure Communication Links
- High Speed Digital Links
- Wireless Security
- Digital Cordless Telephones

Product Description

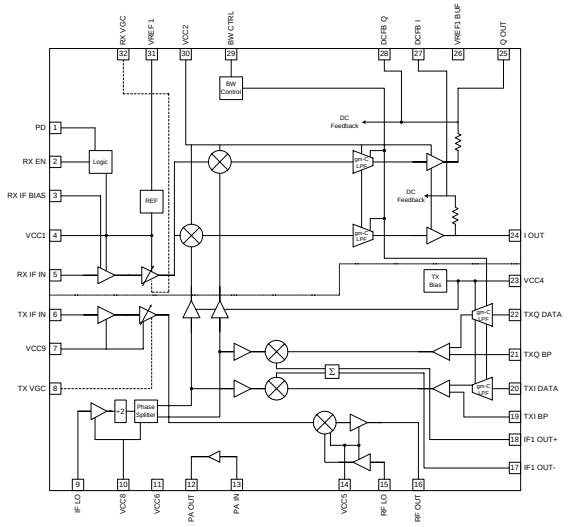
The RF2948B is a monolithic integrated circuit specifically designed for direct-sequence spread-spectrum systems operating in the 2.4GHz ISM band. The part includes: a direct conversion from IF receiver with variable gain control; quadrature demodulator; I/Q baseband amplifiers; and, on-chip programmable baseband filters. For the transmit side, a QPSK modulator and upconverter are provided. The design reuses the IF SAW filter for transmit and receive reducing the number of SAW filters required. Two-cell or regulated three-cell (3.6V maximum) battery applications are supported by the part. The part is also designed to be part of a 2.4GHz chipset consisting of the RF2494 LNA/Mixer, one of the many RFMD high-efficiency GaAs HBT PA's and the RF3000 Baseband Processor.



Package Style: QFN, 32-Pin, 5x5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ InGaP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☐ Si CMOS
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- 45MHz to 500MHz IF Quad Demod
- On-Chip Variable Baseband Filters
- Quadrature Modulator and Upconverter
- 2.7V to 3.6V Operation
- Part of IEEE802.11b Chipset
- 2.4GHz PA Driver

Ordering Information

RF2948B	2.4GHz Spread-Spectrum Transceiver
RF2948BTR13	2.4GHz Spread-Spectrum Transceiver (Tape & Reel)
RF2948B PCBA	Fully Assembled Evaluation Board

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Greensboro, NC 27409, USA
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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+12	dBm
LO Input Levels	+5	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

MSL JEDEC level 3 at 240°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

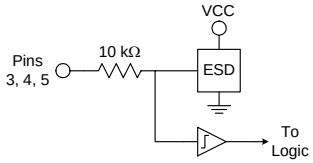
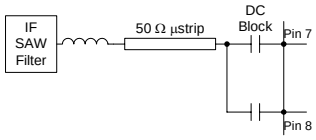
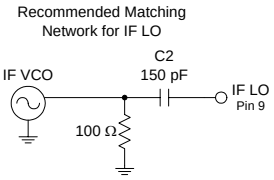
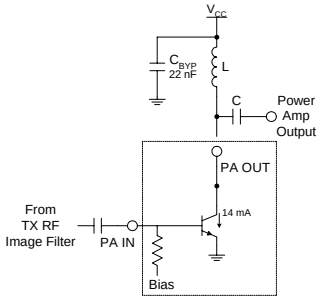
Refer to "Soldering Specifications" on page 16-13 for special soldering information.

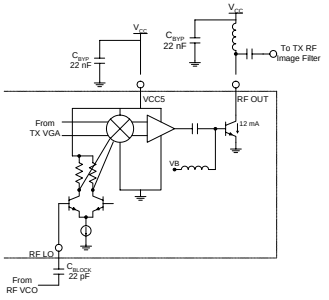
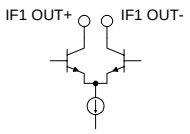
Caution! ESD sensitive device.

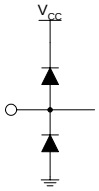
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Receiver					T=25°C, V_{CC}=3.0V, Freq=374MHz, R_{BW}=10kΩ
RX Frequency Range	45	374	500	MHz	
Cascaded Voltage Gain	65		76	dB	RX V_{GC}=1.2V
	0		3	dB	RX V_{GC}=2.0V
Cascaded Noise Figure	5.5		35.0	dB	Varies with gain.
Cascaded Input IP3		50		dBμV	V_{GC} <1.2V
Cascaded Input IP3		115		dBμV	V_{GC}>2.0V
IF LO Leakage		-68		dBm	f=374MHz, LO Power=-10dBm
Quadrature Phase Variation		0	±3	°	With expected LO amplitude and harmonic content.
Quadrature Amplitude Variation		0	±1	dB	
Output P1dB	1.2			V_{PP}	1.4<RX V_{GC}<1.8V
Distortion			2	%	At 0.70V_{PP} output level.
IF AMP and Quad Demod					
Gain		4.5	7.5	dB	V_{GC}=1.95V=min gain
	65	70			V_{GC}=1.25V max gain
Noise Figure		5.5		dB	Single Sideband, max gain.
IF Input Impedance		515-j994		Ω	Single-ended. 374MHz
RX Baseband Amplifiers					
THD		2		%	At 0.707V_{P-P} output level
Output Voltage		700		mV_{PP}	R_L≥5kΩ, C_L≤15pF
DC Output Voltage	VREF1-15	VREF1	VREF1+15	mV	
RX Baseband Filters					
Baseband Filter 3dB Bandwidth	1	10	35	MHz	5th order Bessel LPF. Set by BW CTRL (RBW)
Passband Ripple			0.1	dB	
Baseband Filter 3dB Frequency Accuracy		±10	±30	%	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Baseband Filter Ultimate Rejection		>80		dB	
Output Impedance		20		Ω	Designed to drive≥5kΩ, ≤15pF load.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Modulator and LPF					
Filter Gain		0		dB	Any setting
Baseband Filter 3dB Bandwidth	1		35	MHz	5th order Bessel LPF, Set by BW CTRL
Passband Ripple			0.1	dB	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Ultimate Rejection		>80		dB	
Input Impedance	3			kΩ	Single-ended
Input AC Voltage		100		mV_{p-p}	Linear, Single-ended.
Input P1dB	200			mV_{p-p}	Single-ended.
Input DC Offset Requirement	1.6	1.7	1.8	V	For correct operation.
IF Frequency Range	45		500	MHz	
Differential Output Resistance		22		kΩ	Between output pins. Open collector when TX on, Hi Z when TX off
Differential Output Capacitance		0.436		pF	Between output pins.
Shunt Output Capacitance		0.4		pF	From each pin to ground.
I/Q Phase Balance		0	±3		
I/Q Gain Balance		0	±1	dB	
Conversion Transconductance		0.0185		S	Single-ended voltage input to differential output current conversion gain.
Carrier Output	-18	-26		dBc	Without external offset adjustments. 374MHz. Compared to modulated signal, 100mV_{P-P} input.
Harmonic Outputs		-30		dBc	
Transmit VGA and Upconverter					
VGA Gain Range		17		dB	
VGA Control Voltage Range		1.0 to 2.0		V	Positive Slope
VGA Gain Sensitivity		17		dB/V	
VGA Input Impedance		515-j994		Ω	374MHz
RF Mixer Output Impedance		50		Ω	With matching elements.
VGA/Mixer Conversion Gain		-3 to +14		dB	With 50Ω match on the output.
VGA/Mixer Output Power		-9		dBm	1dB compression - Single Sideband, TX GC=1.0V. (Desired signal power)
VGA/Mixer Output Power		-4		dBm	1dB compression - Single Sideband, TX GC=2.0V. (Desired signal power)

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Power Amp					
Linear Output Power		6		dBm	
Gain		9		dB	
Output P1dB	10	12		dBm	
Output Impedance		50		Ω	Nominal
Input Impedance		50		Ω	Nominal
Power Down Control					
Logical Controls “ON”	V_{CC}-0.3V		V_{CC}+0.3V	V	Voltage supplied to the input, not to exceed 3.6V.
Logical Controls “OFF”	-0.3	0	0.3	V	Voltage supplied to the input.
Control Input Impedance		>1		MΩ	
RX V_{GC} Response TIme		200		ns	Full step in gain, to 90% of final output level.
RX EN Response TIme		2		μs	I/Q output VALID
TX EN Response TIme		330		ns	To IF output VALID
V_{PD} to RX Response TIme		1.33		ms	To I/Q output VALID
V_{PD} to TX Response TIme		50		μs	To IF output VALID
IF LO Input					The IF LO is divided by 2 and split into quadrature signals to drive the frequency mixers.
Input Impedance		1050-j1200		Ω	f=748MHz
Input Power Range	-15	-10	0	dBm	peak
Input Frequency	90		1000	MHz	(2x IF Frequency)
RF LO Input					
Input Impedance		33-j110		Ω	f=2.04GHz unmatched.
Input Power Range	-10		0	dBm	
Input Frequency	2000		2400	MHz	
VREF1 Buffered					
Source/Sink Current			1	mA	
Output Voltage	VREF1-10		VREF1+10	mV	
VREF1	1.6	1.7	1.8	V	
Power Supply					
Voltage	2.7	3.3	3.6	V	
Total Current Consumption					V_{CC}=3.3V, Baseband BW 1MHz to 40MHz
Sleep Mode Current		1		μA	PD=0, RX EN=1
PA Driver Current		18		mA	TX EN=1
RX Current BW (MHz)					
9		65	85	mA	
12-20		70		mA	
20-30		110		mA	
TX Current BW (MHz)					
9		95	136	mA	
12-20		105		mA	
20-30		115		mA	

Pin	Function	Description	Interface Schematic
1	PD	This pin is used to power up or down the transmit and receive baseband sections. A logic high powers up the quad demod mixers, TX and RX GmC LPF's, baseband VGA amps, data amps, and IF LO buffer amp/ phase splitter. A logic low powers down the entire IC for sleep mode. Also, see State Decode Table.	
2	RX EN	Enable pin for the receiver 15dB gain IF amp and the RX VGA amp. Powers up all receiver functions when PD is high, turns off the receiver IF circuits when low. Also, see State Decode Table. When this pin is a logic "high", the device is in receive mode. When this pin is a logic "low", the device is in transmit mode.	See pin 1.
3	RX IF BIAS	Shunt resistor of 23.7±1% to ground. Biases IF AMPS.	
4	VCC1	Power supply for RX VGA amplifier, IC logic and RX references.	
5	RX IF IN	IF input for receiver section. Must have DC-blocking cap. The capacitor value should be appropriate for the IF frequency. For half-duplex operation, connect RX IF IN and TX IF IN signals together after the DC blocking caps, then run a transmission line from the output of the IF SAW. AC coupling capacitor must be less than 150pF to prevent delay in switching RX to TX/TX to RX.	See pin 6.
6	TX IF IN	Input for the TX IF signal after SAW filter. External DC-blocking cap required. For half-duplex operation, connect RX IF IN and TX IF IN signals together after the DC-blocking caps, then run a transmission line from the output of the IF SAW. AC coupling capacitor must be less than 150pF to prevent delay in switching RX to TX/TX to RX.	
7	VCC9	Power supply for the TX 15dB gain amp and TX VGA.	
8	TX VGC	Gain control setting for the transmit VGA. Positive slope.	
9	IF LO	IF LO input. Must have DC-blocking cap. The capacitor value should be appropriate for the IF frequency. LO frequency=2xIF. Quad mod/demod phase accuracy requires low harmonic content from IF LO, so it is recommended to use an n=3 LPF between the IF VCO and IF LO. This is a high impedance input and the recommended matching approach is to simply add a 100Ω shunt resistor at this input to constrain the mismatch.	
10	VCC8	Power supply for IF LO buffer and quadrature phase network.	
11	VCC6	Power supply for transmitter bias generator.	
12	PA OUT	This is the output transistor of the power amp stage. It is an open collector output. The output match is formed by an inductor to V_{CC}, which supplies DC and a series cap.	

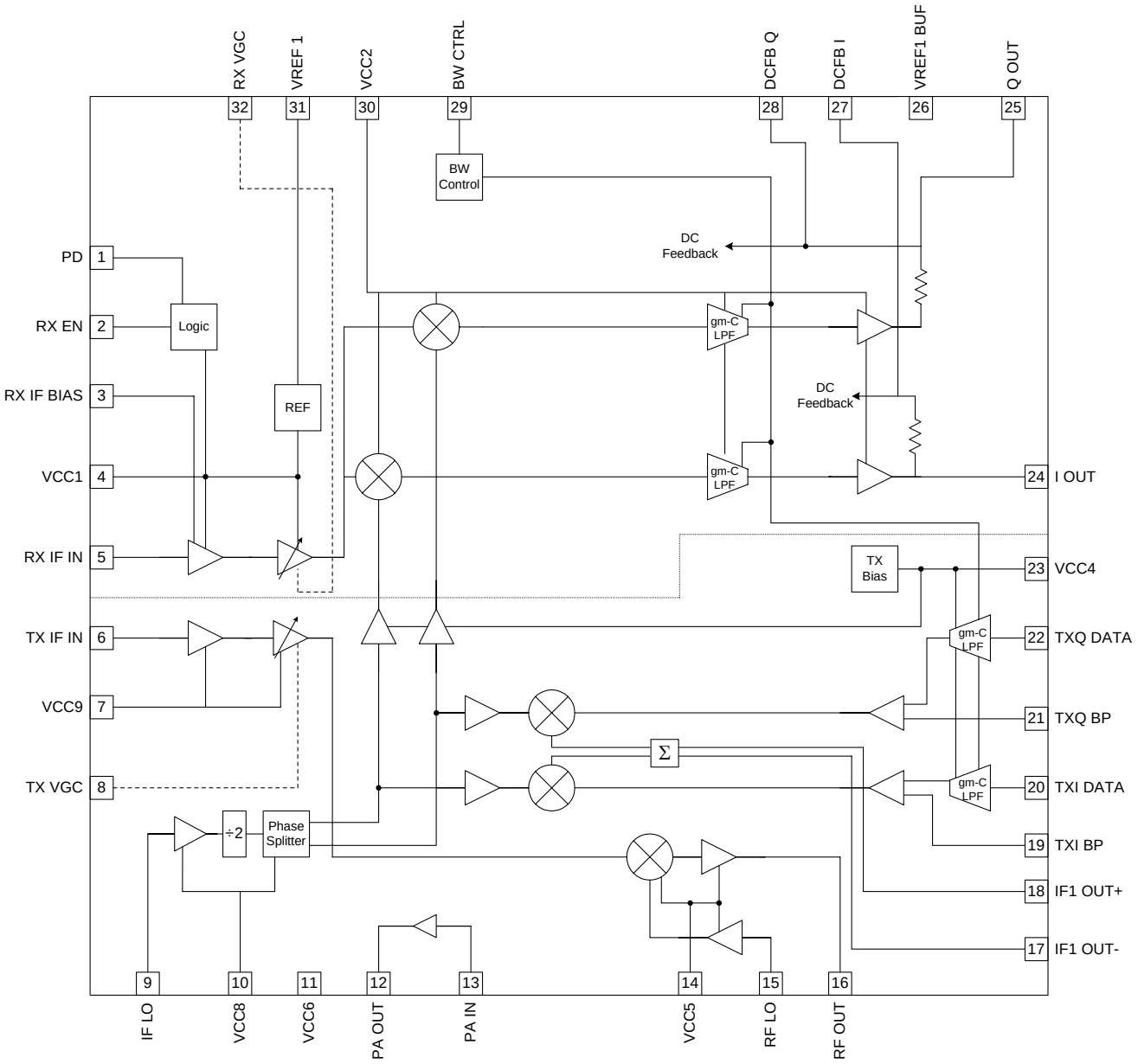
Pin	Function	Description	Interface Schematic
13	PA IN	Input to the power amplifier stage. This is a 50Ω input. Requires DC-blocking/tuning cap.	See pin 12.
14	VCC5	Supply for the RF LO buffer, RF upconverter and amplifier.	
15	RF LO	Single-ended LO input for the transmit upconverter. External matching to 50Ω and a DC-block are required.	See pin 14.
16	RF OUT	Upconverted Transmit signal. This 50Ω output is intended to drive an RF filter to suppress the undesired sideband, harmonics, and other out-of-band mixer products.	See pin 14.
17	IF1 OUT-	The inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT+, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT-.	
18	IF1 OUT+	The non-inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT-, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT+.	See pin 17.
19	TXI BP	This is the in-phase modulator bypass pin. A 10nF capacitor to ground is recommended.	
20	TXI DATA	I input to the baseband 5 pole Bessel LPF for the transmit modulator.	
21	TXQ BP	This is the quadrature phase modulator bypass pin. A 10nF capacitor to ground is recommended.	
22	TXQ DATA	Q input to the baseband 5 pole Bessel LPF for the transmit modulator.	
23	VCC4	Power supply for quadrature modulator.	
24	I OUT	Baseband analog signal output for in-phase channel. 700mV$_{P-P}$ linear output.	
25	Q OUT	Baseband analog signal output for quadrature channel. 700mV$_{P-P}$ linear output.	
26	VREF1 BUF	Buffered version of the VREF1 output. See pin 31. Sink/Source current <1mA.	
27	DCFB I	DC feedback capacitor for in-phase channel. Requires capacitor to ground. (22nF recommended)	
28	DCFB Q	DC feedback capacitor for quadrature channel. Requires decoupling capacitor to ground. (22nF recommended)	
29	BW CTRL	This pin requires a resistor to ground to set the baseband LPF bandwidth of the receiver and transmit GmC filter amps.	
30	VCC2	Supply for the I and Q baseband and GmC filters. This pin should be bypassed with a 10nF capacitor.	

Pin	Function	Description	Interface Schematic
31	VREF 1	This is a bypass pin for the bias circuits of the GmC filter amps and for I/Q inputs. No current should be drawn from this pin (<10μA). 1.7V nominal.	
32	RX VGC	Receiver IF and baseband amp gain control voltage. Negative slope.	
Pkg Base		Ground for all circuitry in the device. A very low inductance from the base to the PCB groundplane is essential for good performance. Use an array of vias immediately underneath the device.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1-4, 7, 8, 10, 19-32.	

State Decode Table	Input Pins		Internally Decoded Signals		
	PD	RX EN	BB EN	RXIF EN	TXRF EN
Sleep Mode	0	x	0	0	0
Receive Mode	1	1	1	1	0
Transmit Mode	1	0	1	0	1

NOTES	
BB_EN Enables:	
	TX_LPF's and buffers
	Quad Demodulator mixers
	Baseband Amps and gm-C LPF's
	IF LO buffer/phase splitters
RXIF_EN Enables:	
	Front-end IF amplifier (RX)
	RX IF VGA amplifiers
TXRF_EN Enables:	
	Front-end IF amplifier (TX)
	TX VGA
	RF upconverter and buffer
	PA driver
	RF LO buffer
	Quad Modulator mixers

Detailed Functional Block Diagram



Theory of Operation

RECEIVER

RX IF AGC/Mixer

Being essentially high impedance, RX IF IN responds to the input voltage (rather than power), and amplifies that voltage by the gain specified in the datasheet, then presents the output voltage at a high impedance (after downconversion). For characterization purposes, a 50Ω shunt resistor is placed on the IF signal path, before AC-coupling to the input. A 50Ω signal source is applied directly across the shunt resistor, through a coaxial test lead. The signal source sees the shunt resistor and therefore a low SWR. Voltage gain is then simply the ratio of the output voltage to the input voltage.

The front end of the IF AGC starts with a single-ended input and a constant gain amp of 15dB. This first amp stage sets the noise figure and input impedance of the IF section, and its output is taken differentially. The rest of the signal path is differential until the final baseband output, which is converted back to single-ended. Following the front end amp are multiple stages of variable gain differential amplifiers, giving the IF signal path a gain range of 4.0dB to 70.0dB. The noise figure (in max gain mode) of the IF amplifiers is 5dB, which should not degrade the system noise figure.

The IF to BB mixers are double-balanced, differential in, differential out, mixers with negligible conversion gain. The LO for each of these mixers is shifted 90° so that the I and Q signals are separated in the mixers.

RX Baseband Amps, Filters, and DC Feedback

At baseband frequency, there are fully integrated gm-C low pass filters to further filter out-of-band signals and spurs that get through the SAW filter, anti-alias the signal prior to the A/D converter, and to band-limit the signal and noise to achieve optimal signal-to-noise ratio. The 3dB cut-off frequency of these low pass filters is programmable with a single external resistor, and continuously variable from 1MHz to 35MHz. A five-pole Bessel type filter response was chosen because it is optimal for data systems due to its flat delay response and clean step response. Butterworth and Chebychev type filters ring when given a step input making them less ideal for data systems. The filter outputs drive the linear 700mV$_{PP}$ signal off-chip.

DC feedback is built into the baseband amplifier section to correct for input offsets. Large DC offsets can arise when a mixer LO leaks to the mixer input and then mixes with itself. DC offsets can also result from random transistor mismatches. A large external capacitor is needed for the DC feedback to set the high pass cutoff.

LO INPUT BUFFERS

RF LO Buffer

The RF LO input has a limiting amplifier before the mixer on both the RF2494 (RX) and RF2948B (TX). This limiting amplifier design and layout is identical on both ICs, which will make the input impedance the same as well. Having this amplifier between the VCO and mixer minimizes any reverse effect the mixer has on the VCO, expands the range of acceptable LO input levels, and holds the LO input impedance constant when switching between RX and TX. The LO input power range is -18dBm to +5dBm, which should make it easy to interface to any VCO and frequency synthesizer.

IF LO Buffer

The IF LO input has a limiting amplifier before the phase splitting network to amplify the signal and help isolate the VCO from the IC. Also, the LO input signal must be twice the desired intermediate frequency. This simplifies the quadrature network and helps reduce the LO leakage onto the RX_IF input pin (since the LO input is now at a different frequency than the IF). The amplitude of this input needs to be between -15dBm and 0dBm. Excessive IF LO harmonic content affects phase balance of the modulator and demodulator so it is recommended that IF LO harmonics be kept below -30dBc.

The PA driver is a one-stage class A amplifier with 10dB gain and capable of delivering 6dBm of linear power to a 50Ω load, and has a 1dB compression point of 12dBm. For lower power applications, this PA driver can be used to drive a 50Ω antenna directly.

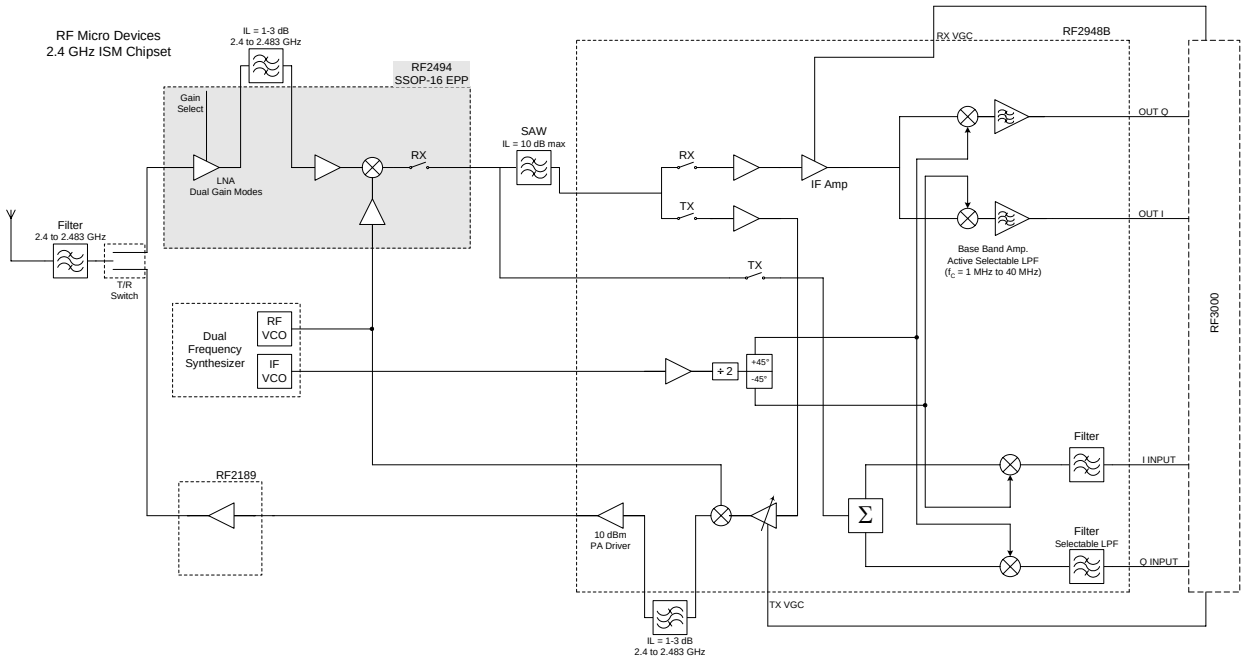
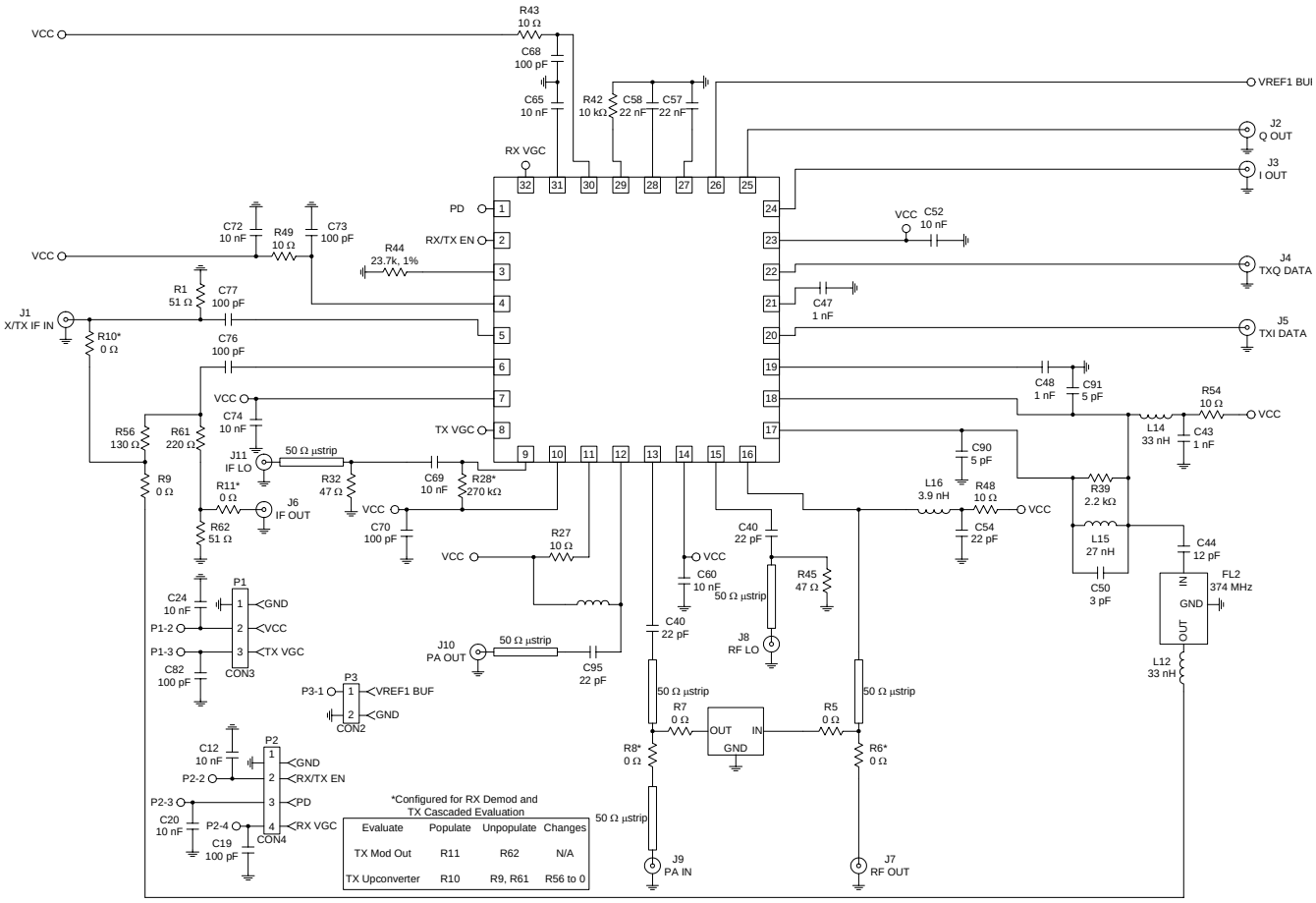


Figure 1. Entire Chipset Functional Block Diagram

Evaluation Board Schematic

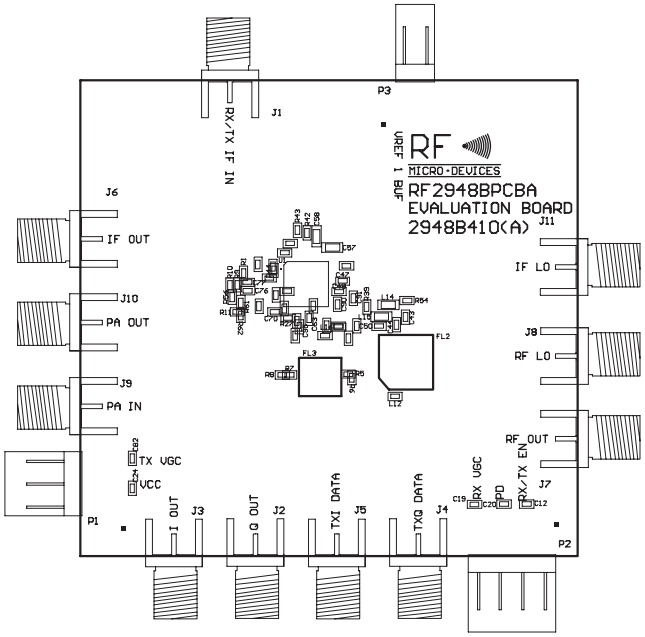


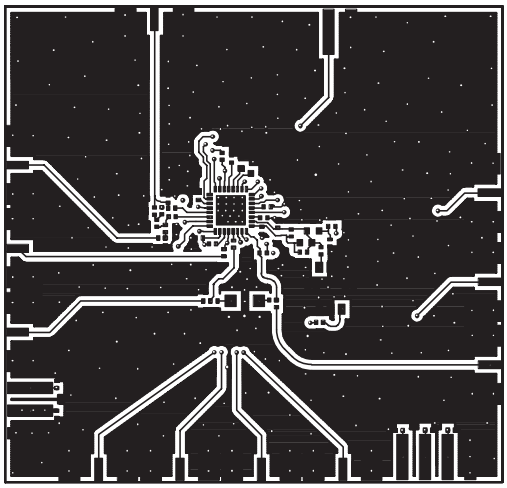
*Configured for RX Demod and TX Cascaded Evaluation

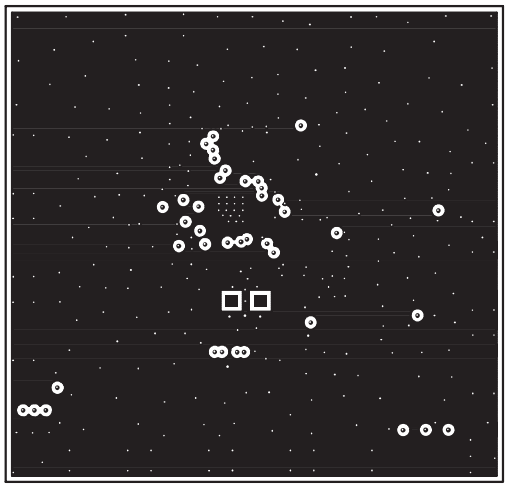
Evaluate	Populate	Unpopulate	Changes
TX Mod Out	R11	R62	N/A
TX Upconverter	R10	R9, R61	R56 to 0

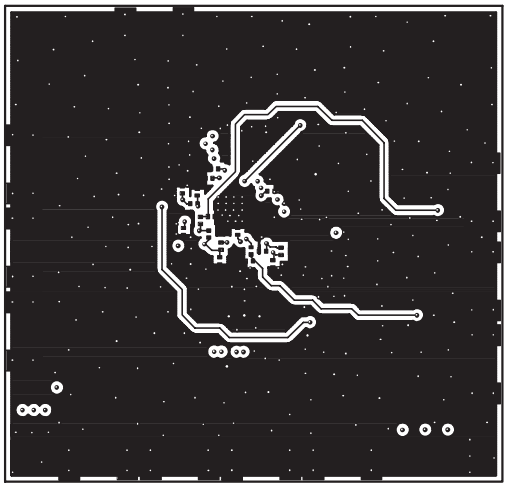
Evaluation Board Layout
Board Size 2.2” x 2.1”

Board Thickness 0.031”, Board Material FR-4, Multi-Layer

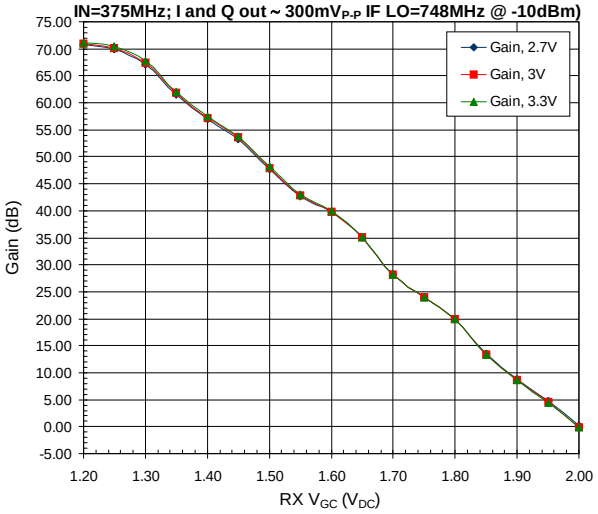




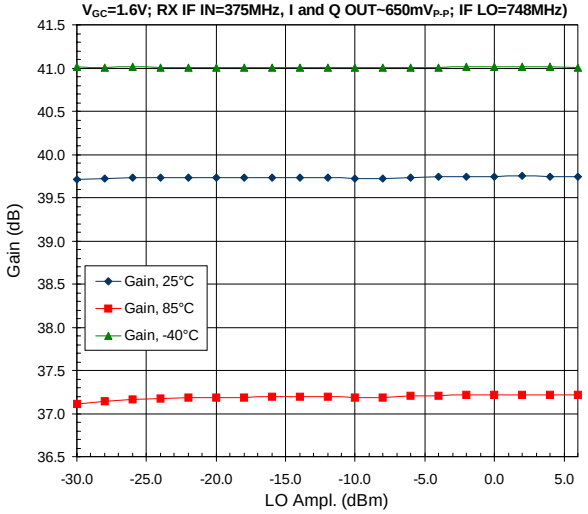




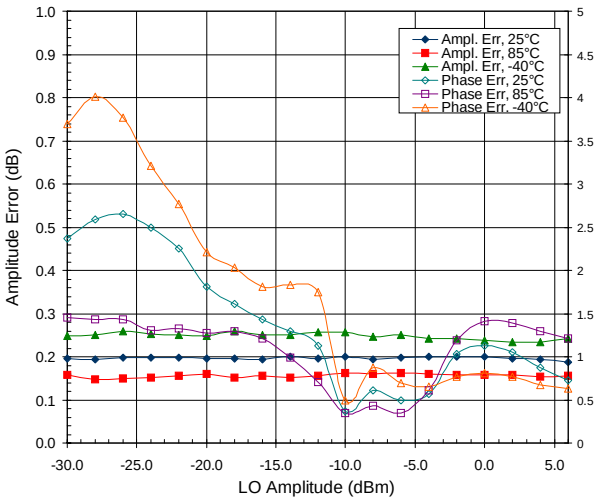
RX Voltage Gain versus V_{GC} and V_{CC} (Temp=25°C; RX IF IN=375MHz; I and Q out ~ 300mV$_{P-P}$ IF LO=748MHz @ -10dBm)



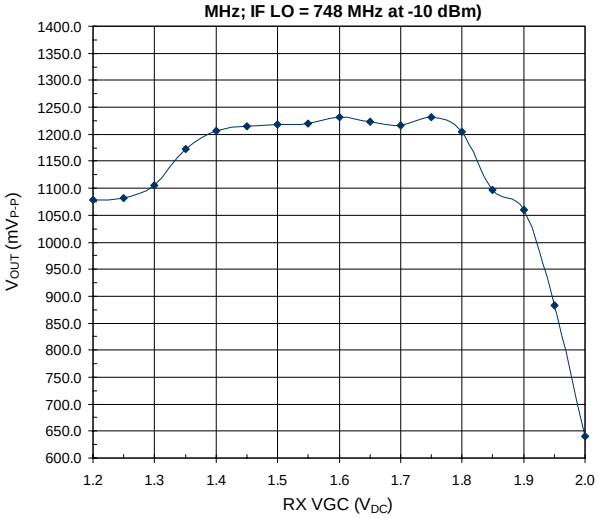
RX Gain versus IF LO Amplitude and Temp (V_{CC}=3V; RX V_{GC}=1.6V; RX IF IN=375MHz, I and Q OUT~650mV$_{P-P}$; IF LO=748MHz)



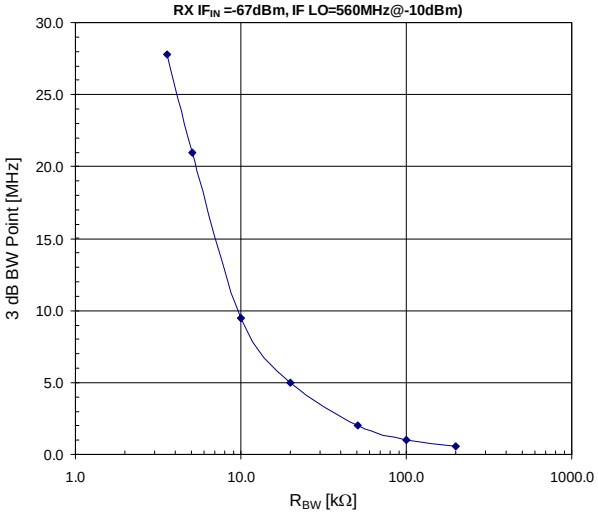
RX IQ Amplitude and Phase Error versus IF LO Amplitude and Temp (V_{CC}=3V; RX V_{GC}=1.6V; RX IF IN=375MHz, I&Q OUT~650mV$_{P-P}$; IF LO=748MHz)



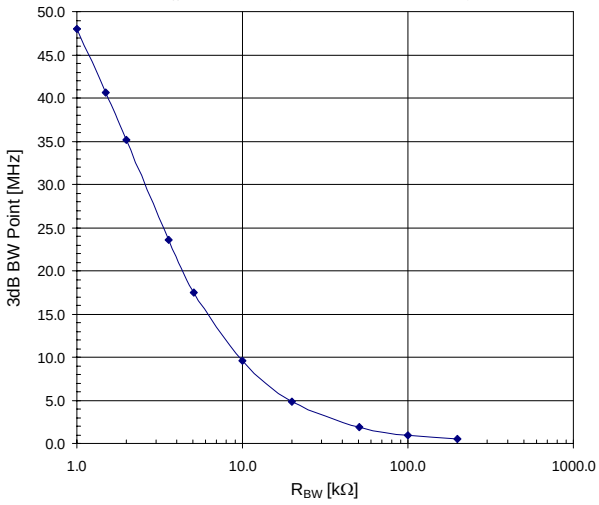
RX OP1dB versus VGC and Temp (V_{CC} = 3 V; RX IF_{IN} = 375 MHz; IF LO = 748 MHz at -10 dBm)



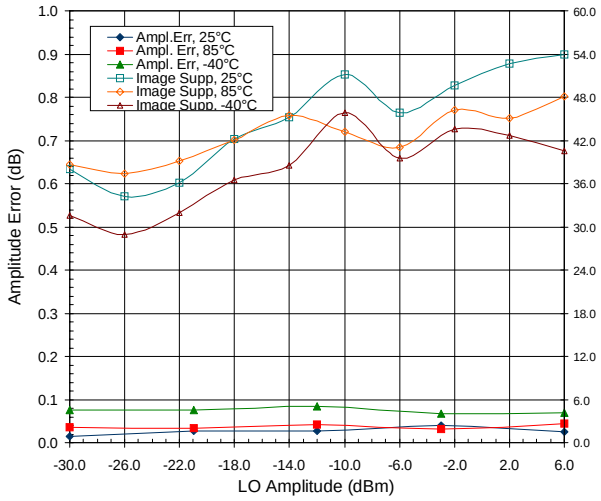
RX 3dB BW versus R_{BW} (Temp=Ambient, V_{CC}=3.15V, V_{GC}=1.6V, RX IF_{IN} =-67dBm, IF LO=560MHz@-10dBm)



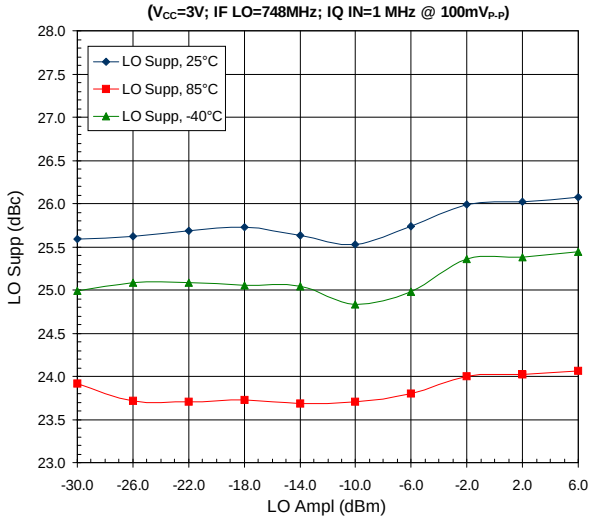
TX 3dB BW Point versus R_{BW} (Broadband 50Ω match on IFOUT, Temp=Ambient, V_{CC}=3.15V, GCTX=1.5V, I&Qin=100mV$_{P-P}$, IFLO=560MHz@-10dBm)



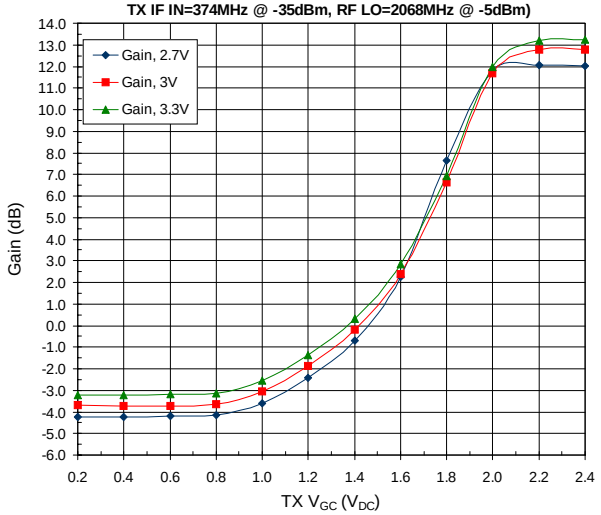
Modulator Amplitude Error and Image Suppression versus IF LO Amplitude and Temp (V_{CC}=3V; IF LO=748MHz; IQ IN=1MHz @ 100mV$_{P-P}$)



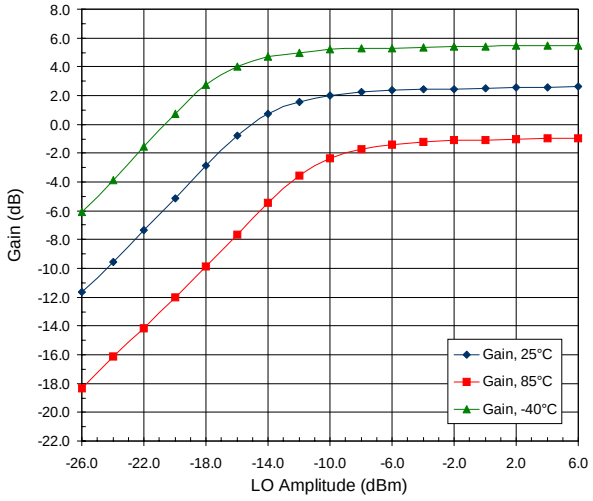
Modulator LO Suppression versus IF LO Amplitude and Temp (V_{CC}=3V; IF LO=748MHz; IQ IN=1 MHz @ 100mV$_{P-P}$)



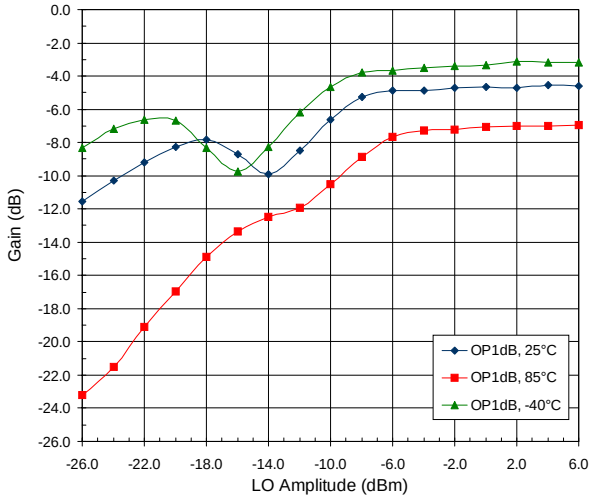
Upconverter Voltage Gain versus V_{GC} and V_{CC} (Temp=25°C; TX IF IN=374MHz @ -35dBm, RF LO=2068MHz @ -5dBm)



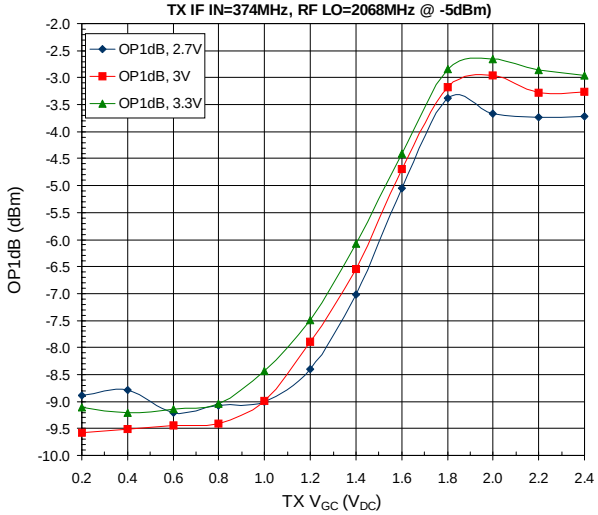
Upconverter Voltage Gain versus RF LO Amplitude and Temp (V_{CC}=3V; TX V_{GC}=1.6V; TX IF IN=374MHz@-35dBm, RF LO=2068MHz)

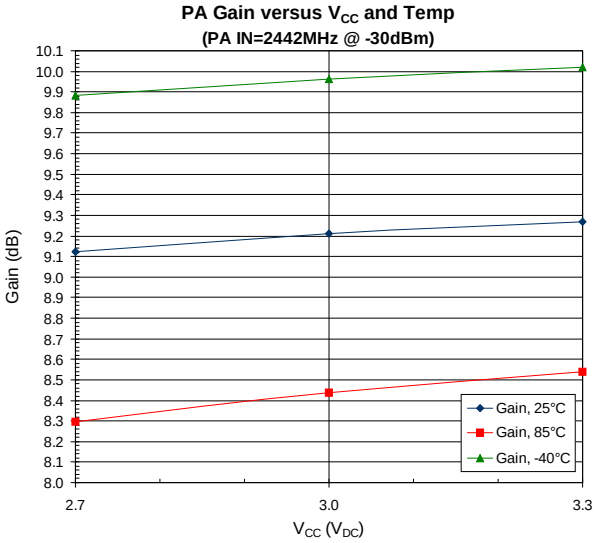


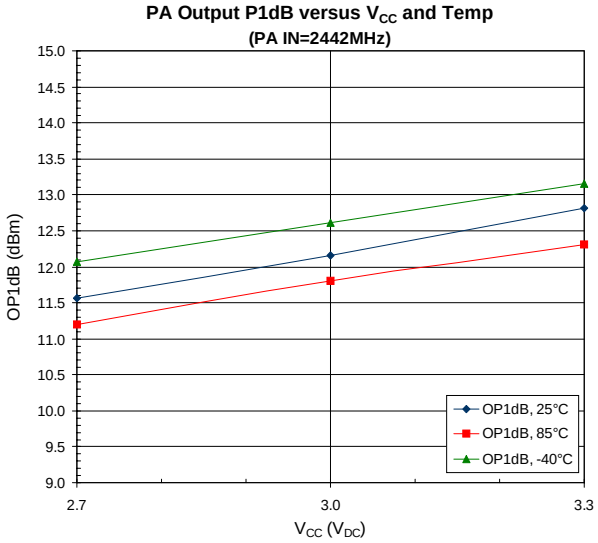
Upconverter Output P1dB versus RF LO Amplitude and Temp (V_{CC}=3V; TX V_{GC}=1.6V; TX IF IN=374MHz, RF LO=2068MHz)



Upconverter Output P1dB versus V_{GC} and V_{CC} (Temp=25°C; TX IF IN=374MHz, RF LO=2068MHz @ -5dBm)




PA Gain versus V_{CC} and Temp
(PA IN=2442MHz @ -30dBm)
Gain (dB)
10.1
10.0
9.9
9.8
9.7
9.6
9.5
9.4
9.3
9.2
9.1
9.0
8.9
8.8
8.7
8.6
8.5
8.4
8.3
8.2
8.1
8.0
2.7
3.0
3.3
V_{CC} (V_{DC})
Gain, 25°C
Gain, 85°C
Gain, -40°C


PA Output P1dB versus V_{CC} and Temp
(PA IN=2442MHz)
OP1dB (dBm)
15.0
14.5
14.0
13.5
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
9.0
2.7
3.0
3.3
V_{CC} (V_{DC})
OP1dB, 25°C
OP1dB, 85°C
OP1dB, -40°C